## REMARKS

The Applicant has amended Claim 1 to include the limitations of now cancelled Claim 5. The additional limitations of Claim 1 can clearly be seen in Figure 5 of the disclosure.

The Applicant has also made clarifying amendments to other claims.

No new matter has been added.

## CLAIM REJECTIONS

The Office has improperly rejected all of the pending claims as being unpatentable over Lee.

On the face of the rejections, the Office has unquestionably failed to establish a prima facie case of obviousness. The Office uses Lee as a general teaching document, stating the claims are within the scope of the disclosure. Obviously, this is not the case, or an anticipation rejection would have been forth coming.

The Office's only specific reference to the Lee document is directed to Figure 17. The Office states that in the array of Figure 17, word lines are tied to the gates of the split-gate memory cell and source lines are tied to the sources of the select gate MOSFET devices. The Office goes on to state that bit lines may be tied to the drains of the split-gate memory cell, and select lines may be tied to the select gates of the select gate MOSFET devices. There is no mention of the voltage scheme to erase and program the cells of the array, only a conclusory statement that "The claimed voltage schemes are also

within the scope of this reference". Furthermore, Figure 17 is actually described in another patent.

The Office is required to show how each element of the present claims is met and if not in the same disclosure, the motivation to combine must be stated. In the present case the Office has simply issued a general rejection citing a 69 page Patent containing a Figure described in a 38 page non cited patent. In no manner can the present rejection meet the requirements of a prima facie case of obviousness. It must be withdrawn or the limitations in the claims specifically addressed as required.

It is also unclear, if the Office is relying on Lee 223 or Lee 538 where Figure 17 is actually described. Lee '223 states "the details of the array architecture can be referred to in Aplus' patent 5,748,538" (Col. 21, lines 61-63). Apart from Figure 17, the structure of the present claims is not shown in Lee, and certainly not highlighted by the Office as required.

Amended Claim 1 recites:

> "A memory array with byte-alterable capability comprising:
>
> a plurality of adjacent cells each comprising,
>
> a select gate metal oxide semiconductor field effect transistor, MOSFET device, and
>
> a split-gate memory cell whose source is connected to the drain of said select gate MOSFET device wherein the gate of said select gate MOSFET device is controlled independently of the gate of said split-gate memory cell
>
> select lines connecting the select gate of the select gate MOSFET device of one of the plurality of adjacent cells to the select gate of the select gate MOSFET device of an adjacent one of the plurality of adjacent cells."

Lee '538 from which Figure 17 is drawn, clearly discloses that adjacent cell have separated select gates. Lee '538 states:

> "In addition, every pair of adjacent transistor cells in the row direction are grouped into first and second sides." (Col. 7, ll. 4-6)
>
> "Referring again to FIG. 4, note that the transistor cells in the column direction have sub-source and sub-bit lines which are not shared with the transistor cells in the adjacent columns." (Col. 8, ll. 1-5)

Therefore, Lee '538 does not disclose select lines connecting the select gates of adjacent cells as recited in Claim 1. This is also readily apparent from Figure 17 of Lee '223 where SC2a of the first cell is independent from SG2b of the second cell likewise for SC1a and SG1b. Each Byte of Lee '223 have adjacent cell with independent select gates. Thus the rejection is improper and must be withdrawn.

Furthermore, as Claims 2-4, 6-18 depend from Claim 1, their rejections are also improper irrespective of any additional subject matter recited therein.

However, in order to further prosecution of the present claims, Lee's additional inapplicability to Claims 12-18 is also discussed.

Claim 12 requires a common source line between the bits, however, from Table I of Lee '538, it is clear that Va and Vb have different voltage values and thus are not common. Additionally, Claim 15 requires a high voltage on the selected gates of the selected bytes for erasure, however Table I indicates the gates at zero (0) voltage.

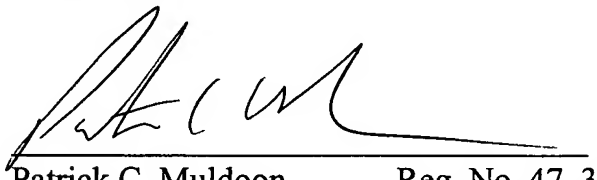
Therefore, it is clear that the structure of Figure 17 is not the same as the structure presently claimed and that all the elements of Claims 12-18 are not found in Lee '223 or '538.

## CONCLUSION

The Office has failed to establish a prima facie case of obviousness. The Office has failed by outright omission to correlate the features of Lee with the claimed elements in the present application. Additionally the elements recited in the claims are not found in either of Lee's disclosures. Therefore, the Applicant requests withdrawal of the rejections and allowance of the application, including Claims 1-4, 6-18.

Although an extension of time is not deemed necessary at this time, the Office is hereby authorized to charge any appropriate extension fee to Deposit Account No. 04-1679, Duane Morris LLP.

Respectfully submitted,



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